International J.of Multidispl.Research & Advcs. in Engg.(IJMRAE),
ISSN 0975-7074, Vol. 3, No. I (January 2011), pp. 411-421

IMPLEMENTATION OF IEEE-754 TO DECIMAL CONVERSION OF LIBRARY COMPONENTS FOR FLOATING POINT ARITHMETIC UNIT

VISHAL KUMAR SRIVASTAVA, K. C. TYAGI, DILEEP KUMAR JAISWAL AND DHEERAJ AGGRAWAL

Abstract

This paper deals with implementation of IEEE-754 to Decimal Conversion using VHDL. This work will minimize the work of the processor unit. Here, we have utilized VHSIC Hardware Description Language and Xilinx to implement this conversion. A floating point processor unit is able to process all the operations on integers as well as on float values or all real values. It first converts the real values in normalized form then performs the different operations. The floating point unit is that part of computer that actually helps the ALU to perform arithmetic and logical operations on data. All of the other elements of the computer system-control unit registers, memory, I/Os are there mainly to bring data into the ALU for it to process and then to take the results back out.

Keywords: IEEE Standard 754, Exponent, Mantissa, Normalized, Denormalized.

© Ascent Publication House: http: //www.ascent-journals.com